Title: **TEST STRUCTURE OF DRAM**

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[0001] This Application claims priority to Taiwan Patent Application No. 092100402 filed on January 09, 2003.

Field of Invention

[0002] The present application relates to a test structure of a semi-conductor, in particular, a test structure of DRAM.

Background of the Invention

[0003] In the process of producing semi-conductor devices, it takes many steps to form the desired devices. In the process of forming DRAM, for example, it takes many steps to form a capacitor and a transistor to build up a memory cell. To ensure the structures are correctly formed on the wafer by those steps, there are usually test structures on the wafers. During the steps, the correctness of the structures of the devices on the wafers is ensured by detecting the electric polarity or other features of the test structure.

[0004] Fig. 1 is a cross-sectional view of a test structure on a wafer using to form a DRAM in the prior art. In a substrate 100, a first deep trench capacitor 102 and a second deep trench capacitor 104 are formed. A first gate contact 110 and a second source/drain 118, 120 form a transistor. A second gate contact 116 and a second source/drain 126, 128 form another transistor. A first buried strap 122 is formed adjacent to the first deep trench capacitor 102. A second buried strap 124 is formed adjacent to the second deep trench capacitor 104. By means of a first contact 106 and a second contact 108, the threshold

voltage Vt of the transistor is detected to check if the structure on the wafer is correct. For example, a drift formed by the contact of the trench and the gate may contribute to the decrease of threshold voltage Vt.

[0005] The active area AA1 in the structure of Fig. 1 is larger than the normal active area of a memory cell. It cannot reflect the actual situation of the active area of a memory cell, and requires to encompass more buried straps. When buried straps have out diffusion effect, the threshold voltage will be affected, too. Subsequently, when using the structure of Fig. 1 to test the structure of DRAMs, the problems on the wafer cannot be identified because too many variables are involved.

Summary of the Invention

[0006] The object of the present invention is to provide a test structure of DRAM, in order to provide a test structure which much more resembles the active area of actual memory cell.

The present invention provides a test structure which is formed on a semi-conductor substrate for DRAM. A transistor is formed on a semi-conductor substrate and includes a first region and a second region, which are formed in the semi-conductor substrate as source/drain of the transistor. A deep trench capacitor, which is formed in the semi-conductor substrate and adjacent to the transistors, has a first width. A shallow trench insulator (STI), which is formed in a top portion of the deep trench capacitor, has a second width. The second width is substantially shorter than the first width. A third region is formed in the semiconductor substrate and adjacent to the deep trench capacitor. A first contact is formed on the semiconductor substrate and is in contact with the first region. A second contact is formed on said semiconductor substrate and is in contact with the third region. By measuring the threshold voltage of the transistor through the first contact and the second contact, whether the structure is correct or not is thus detected.

Brief Description of the Drawings

[0007] Fig. 1 shows the cross-sectional view of a test structure in the prior art.

[0008] Fig. 2 illustrates a test lay-out of DRAM of the present invention.

[0009] Fig. 3 illustrates a cross-sectional view of the test structure of the present invention.

Detailed Description

[0010] The present invention provides a test structure of DRAM on a wafer. The test structure has an active area which much more resembles the actual memory cell to determine if each structure of each step is correctly configured.

[0011] Fig. 2 illustrates a lay-out of test structure of the present invention. Below Active Area 220, a third gate contact 206 and a fourth gate contact 208 are formed. A first deep trench capacitor 224 in the shape of the letter H is formed under the first gate contact 202 and the second gate contact 204. A second deep trench capacitor 226 in the shape of the letter H is formed under the fifth gate contact 210 and the sixth gate contact 212. A first contact 214 is formed on one side of the first gate contact, and a third contact 216 is formed on one side of the sixth gate contact 212. A second gate contact (not shown here) is formed below the Active Area 220 and between the third gate contact 206 and the fourth gate contact 208. Along the cross-sectional line I-I' is the cross-sectional view of the test structure as shown in Fig. 3.

[0012] Along the cross-sectional line I-I' in Fig. 2 is the cross-sectional view of test structure of Fig. 3. The preferable material of semiconductor substrate 300 is silicon. Using a first contact 330 as a border, on semiconductor substrate 300 one device is placed on each side. The two devices on both sides share a first contact 330 and a first region 308. Taking the left device for example, the first region 308 and the second region 310 are formed within semiconductor substrate 300. The first region 308 and the second region 310 act as source/drain regions of the transistor. The third gate contact 322 as well

as a silicon oxide layer 336 is formed on the semiconductor substrate 300. Next, a conduction layer 338 is formed on the silicon oxide layer 336. The conduction layer 338 is preferably made of metal silicide. Third gate contact 322, the first region 308 and the second region 310 make up a transistor.

[0013] As shown in Fig. 3, among the left devices, the deep trench capacitor 302 is formed within the semiconductor substrate 300 and adjacent to the aforesaid transistor. The deep trench capacitor 302 has a first width D1.

[0014] The shallow trench isolation (STI) is formed in a top portion of the deep trench capacitor 302. The STI has a second width D2. As indicated in Fig. 3, the second width D2 is substantially shorter than the first width D2. The structure of the first gate contact 318 and the second gate contact 320 are the same as that of the third gate contact 322, so, no more details are provided here.

[0015] The third region in Fig. 3, being possibly a buried strap, is formed within the semiconductor substrate 300 and adjacent to the first deep trench capacitor 302. The first region 308, the second region 310 and the third region 312 are formed by doping proper dopant(s) into the semiconductor substrate 300. The first contact 330 is formed on the semiconductor substrate 300 and is in contact with the first region 308. The second contact is formed on the semiconductor substrate 300 and is in contact with the third region 308. The gate contact in Fig. 3 is connected to the active word line and the passive word line, respectively. Taking the left device for example, the first gate contact 308 and the second gate contact 320 connect to the passive word line, respectively. The third gate contact 322 connects to the active word line.

[0016] When the test structure in Fig. 3 is used to test the structures of DRAMs on wafers, the first contact 330 and the second contact 332 are used to measure the threshold voltage Vt of the transistor. Once the Vt changes, it indicates that the structures of wafers are

possibly shifted during processing. Decrease of the Vt is caused by the shift of the trench capacitor 302, the first gate contact 318 and the second gate contact 320. The area of the effective region 220 in Fig. 2 and the effective region AA2 in Fig. 3 are the same size as the actual memory cells. In the previous test structure in Fig. 1, the fourth gate contact 116 is moved to overlap with the first gate contact 110 to form the structure in Fig. 3. Compare the test structure in Fig. 3 with the previous one in Fig. 1, two buried straps are cancelled along the test path. The change of Vt can be more sensitively detected due to such modification.

[0017] Because the structure in Fig. 3 is formed by moving the fourth gate contact 116 to overlap with the first gate contact 110 in the previous test structure in Fig. 1, even when the buried strap in the third region 312 causes out diffusion, the charge of the Vt in Active Area AA2 will not be measured.

[0018] The above-mentioned descriptions are mainly focused on the left device in Fig. 3. Since the device on the right side is merely a mirror image of the device on the left side, the similarity of the structures can be easily deduced by persons skilled in the art, and therefore no more details are provided.

[0019] By means of the detailed descriptions of what is presently considered to be the most practical and preferred embodiments of the subject invention, it is the expectation that the features and the gist thereof are plainly revealed. Nevertheless, these above-mentioned illustrations are not intended to be construed in a limiting sense. Instead, it should be well understood that any analogous variation and equivalent arrangement is supposed to be covered within the spirit and scope to be protected and that the interpretation of the scope of the subject invention would therefore as much as broadly apply.